LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method of controlling a data rate in a network, comprising:

placing data packets into a data stream in a network;

routing said data stream through a delay device; and

delaying selected data of the data stream in said network ~~by a fixed delay amount~~ by storing the selected data in memory buffers for a fixed delay amount to control the data rate to increase latency of the network.

2. (Cancelled)

3. (Currently Amended) The method according to claim 1, wherein the fixed delay amount is stored in a configuration table, and said delay device consults the configuration table to determine when to release the selected data from the memory buffers~~includes a configuration table for determining said selected data~~.

4. (Original) The method according to claim 1, wherein said delay causes a change in round trip latency for said selected data.

5. (Original) The method according to claim 1, wherein said network includes at least one client processor, at least one server processor, at least one network router and a delay processor.

6. (Currently Amended) An apparatus for controlling a data rate in [[the]]a network, comprising:

at least one first processor connected to said network;

at least one second processor connected to said network; and

a delay processor for controlling the data rate in said network, the delay processor being operative to store data packets in a plurality of memory buffers for a fixed amount of time and releasing the data packets after the fixed amount of time to increase latency of the network.

7. (Original) The apparatus according to claim 6, wherein said network further comprises at least one router.

8-9. (Cancelled)

10. (Currently Amended) The apparatus according to claim [[9]]6, wherein the fixed amount of time is stored in a configuration table, the delay processor consulting the configuration table to determine when to release the data packets from the memory buffers~~is determined from a configuration table in said delay processor~~.

11. (Currently Amended) A method of controlling a data rate in a network, comprising:

placing data packets into a data stream in a network;

routing said data stream through a delay device; and

delaying data in said network by storing the data in memory buffers for a fixed delay amount to control the data rate to increase latency of the network, the data being delayed by a varying delay amount that is slowly adjusted over time~~determined~~ by passing the data rate through a low pass filter.

12-13. (Cancelled)

14. (Original) The method according to claim 11, wherein said delay causes a change in round trip latency.

15. (Original) The method according to claim 11, wherein said network includes at least one client processor, at least one server processor, at least one network router and a delay processor.

16. (Currently Amended) An apparatus for controlling a data rate in the network, comprising:

at least one first processor connected to said network;

at least one second processor connected to said network; and

a delay processor for controlling the data rate in said network, said delay processor delaying data in said network by storing the data in memory buffers and releasing the data after a

delay, the amount of the delay being variably controlled by the output of the low pass filter, where the low pass filter receives the data rate as an input.

17. (Currently Amended) The apparatus according to claim [[11]]16, wherein said network further comprises at least one router.

18. (Cancelled)

19. (New) The method according to claim 1, further comprising determining the selected data of the data stream by employing a packet selection list that indicates which of the data packets are to be the delayed selected data.

20. (New) The method according to claim 1, further comprising determining the amount of time the selected data is stored in the memory buffers based on an amount of delay stored in a configuration table.

21. (New) The method according to claim 20, further comprising updating the configuration table to change the amount of delay stored in the configuration table upon the delay device receiving a configuration table packet.

22. (New) The method according to claim 1, further comprising storing a release time in the memory buffers along with the selected data, the release time corresponding to a time at which the selected data is to be released from the memory buffers.

23. (New) The apparatus according to claim 6, wherein the delay processor comprises a packet selection list that indicates which of the data packets are to be delayed through the delay processor.

24. (New) The apparatus according to claim 6, wherein the delay processor comprises a clock circuit and a controller operative to determine the fixed amount of time the data packets are stored in the memory buffers based on an amount of delay stored in a configuration table.

25. (New) The apparatus according to claim 24, wherein the controller stores a release time in the memory buffers along with the data packets, the release time corresponding to a time at which the data packets are to be released from the memory buffers by the controller.

26. (New) The method according to claim 11, further comprising determining which of the data of the data stream to be delayed by employing a packet selection list that indicates which of the data packets are to be the delayed data.

27. (New) The method according to claim 11, further comprising:

storing the varying delay amount in a configuration table; and

determining the amount of time the delayed data is stored in the memory buffers based on the varying delay amount stored in the configuration table.

28. (New) The method according to claim 11, further comprising storing a release time in the memory buffers along with the delayed data, the release time corresponding to a time at which the delayed data is to be released from the memory buffers.

29. (New) The apparatus according to claim 16, wherein the delay processor comprises a packet selection list that indicates which of the data is to be delayed.

30. (New) The apparatus according to claim 16, wherein the delay processor comprises a clock circuit and a controller operative to determine the amount of time the data is stored in the memory buffers based on the variably controlled amount of delay being stored in a configuration table.

31. (New) The apparatus according to claim 30, wherein the controller stores a release time in the memory buffers along with the data, the release time corresponding to a time at which the data is to be released from the memory buffers by the controller.